

Metrology for 2D materials-based non-volatile memory concepts

Umberto Celano

¹School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ, 85287 USA

The continuous advances of nanoelectronics device technology are creating an ever-increasing demand for customized materials inside future chips including two-dimensional (2D) materials.[1] Here, the advancement of this class of materials hinges on the development of robust and reliable metrology techniques for electrical characterization, particularly those suitable for large-scale production. The advent of 2D materials in chip manufacturing brings new opportunities for non-volatile memory concepts, as well as new challenges for large-area synthesis, integration, and metrology.[2] A key challenge is the need for techniques that are compatible with wafer-scale fabrication and in-line processing, as these are essential for translating laboratory discoveries into commercial products. Here, I will revise some of the most recent developments for large-area an automated material screening and discuss the tomographic reconstruction of confined volumes for 2D materials-based non-volatile memory devices.

References

- [1] Wei et al., iScience, 25, 10, 105160, 2022
- [2] Celano et al., Nanoscale Adv., 6, 2260, 2024

*Corresponding author: Umberto.celano@asu.edu